16. A read interface circuit comprising:

an input buffer configured to receive data from at least one memory device;

a data receiving memory configured to store the received data transmitted from the input buffer in accordance with a data clock signal; and

a clean data strobe signal generating circuit configured to receive a differential data strobe signal from the at least one memory device, and generate a clean data strobe signal, the clean data strobe signal used as the data clock signal.

17. The read interface circuit of claim **16**, wherein

the clean data strobe signal generating circuit includes a first receiver, a second receiver, and a gate signal generator;

the received differential data strobe signal includes a first input data strobe signal and a second input data strobe signal;

the first receiver configured to receive the first input data strobe signal and the second input data strobe signal and output a first single ended data strobe signal;

the second receiver configured to receive the second input data strobe signal and a reference voltage signal and output a second single ended data strobe signal;

the gate signal generator configured to receive the first and second single ended data strobe signals and generate a data strobe gate signal based on the received first and second single ended data strobe signals; and

the clean data strobe signal is further configured to generate the clean data strobe signal based on the data strobe gate signal and the first single ended data strobe signal.

18. The read interface circuit of claim **16**, wherein the at least one memory device is a volatile semiconductor device.

19. The read interface circuit of claim **16**, wherein the at least one memory device is a non-volatile semiconductor memory device.

20. The read interface circuit of claim **16**, wherein the data receiving memory is further configured to output the stored read data to a memory controller.

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